Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising a source region, a channel region, a drain region, a gate electrode disposed above the channel region, and a two-part drift region disposed adjacent to the channel region and extending to and below the drain region,

wherein a first part of said drift region is formed shallowly at least below at least a substantial part of the gate electrode, and said first part has substantially uniform depth under said gate, wherein the entire first part of said drift region is located below said gate electrode;

wherein a second part of said drift region, having substantially uniform depth, is formed more deeply than said first part and is located below ~~in a neighborhood of~~ the drain region.

2. (Currently Amended) A semiconductor device comprising:

a first conductivity type well region formed in a first conductivity type semiconductor substrate;

a gate electrode formed on the substrate via a gate insulating film;

a first conductivity type body region formed to be adjacent to the gate electrode;

a second conductivity type source region and a channel region formed in the first conductivity type body region;

a second conductivity type drain region formed at a position remote from the first conductivity type body region; and

a two-part, second conductivity type drift region, with a first part having substantially uniform depth formed shallowly from the channel region to the drain region, at least below a substantial part of the gate electrode, wherein the entire first part of said drift region is located below said gate electrode, and a second part of said drift region below ~~in a neighborhood of~~ the

drain region, said second part having substantially uniform depth and being formed more deeply than said first part.

3. (Previously Presented) A semiconductor device according to claim 2, wherein the second conductivity type drift region is doped with

at least two kinds of second conductivity type impurities which have different diffusions coefficients, and

at least one kind of first conductivity type impurity which has a diffusion coefficient substantially equal to or larger than the diffusion coefficient of at least one kind of second conductivity type impurity; and

the first conductivity type impurity cancels the second conductivity type impurities in the region below said shallowly formed first part.

4. (Previously Presented) A semiconductor device according to claim 3, wherein arsenic and phosphorus are the second conductivity type impurities and boron is the first conductivity type impurity.

5-7 (cancelled)

8. (Currently Amended) A semiconductor device comprising a first MOS transistor having a source region, a channel region, a drain region, a gate electrode formed on the channel region, and a drift region formed between the channel region and the drain region, and a second MOS transistor having a source region, a channel region, a drain region, and a gate electrode formed on the channel region,

wherein the drift region of the first MOS transistor is formed shallowly at a uniform depth at least below a substantial part of the gate electrode but formed more deeply below ~~in a neighborhood of~~ the drain region, wherein substantially the entire shallow part of said drift region is located below said gate electrode, and

a source/drain region of the second MOS transistor consists of a low concentration source-drain region, a high concentration source-drain region, and a middle concentration source/drain region whose concentration is higher than that of the low concentration source/drain region but lower than that of the high concentration source/drain region.

9. (Currently Amended) A semiconductor device comprising a first MOS transistor and a second MOS transistor formed on a first conductivity type semiconductor substrate;

wherein the first MOS transistor includes,

a first conductivity type well region formed in the semiconductor substrate,

a first gate electrode formed on the first conductivity type well region via a first gate insulating film,

a first conductivity type body region formed to be adjacent to the first gate electrode,

a second conductivity type source region and a channel region formed in the first conductivity type body region,

a second conductivity type drain region formed at a position remote from the first conductivity type body region, and

a second conductivity type drift~~,~~ region formed from the channel region to the drain region, said second conductivity type drift region being formed shallowly at least below a substantial part of the gate electrode, and formed more deeply below ~~in a neighborhood of~~ the drain region, wherein substantially the entire shallow part of said drift region is located below said gate electrode, and

wherein the second MOS transistor includes,

a second conductivity type well region formed in the semiconductor substrate,

a second gate electrode formed on the second conductivity type well region via a second gate insulating film, and

a source/drain region consisting of a low concentration source/drain region formed to be adjacent to the second gate electrode, a high concentration source/drain region, and a middle concentration source/drain region whose concentration is higher than that of the low

concentration source/drain region but lower than that of the high concentration source/drain region.

10. (Original) A semiconductor device according to claim 9, wherein the first MOS transistor consists of an N-channel LDMOS transistor, and the second MOS transistor consists of a P-channel high breakdown voltage MOS transistor.

11. –16. (Cancelled)

17. (Original) A semiconductor device according to claim 1, wherein the semiconductor device is arranged in plural via a element isolation film, and

a channel stopper layer is formed under the element isolation film.

18. (Cancelled)

19. (Previously Presented) A semiconductor device according to claim 2, wherein the second conductive type drift region is adjacent to the first conductive type body region.

20. – 21. (Cancelled)

22. (Previously Presented) A semiconductor device in accordance with claim 1, wherein the dopant concentration of said first part is higher than that of said second part.

23. (Previously Presented) A semiconductor device in accordance with claim 2, wherein the dopant concentration of said first part is higher than that of said second part.

24. (Previously Presented) A semiconductor device in accordance with claim 4, wherein the arsenic is implanted in the semiconductor substrate by an accelerating voltage of about 160 KeV at a dose of $3x10^{12}/cm^2$.

25. (Previously Presented) A semiconductor device in accordance with claim 8, wherein the low concentration source/drain region is formed by implanting boron in the semiconductor substrate at an accelerating voltage of about 80 KeV at a dose of $8x10^{12}/cm^2$.

26. (Previously Presented) A semiconductor device in accordance with claim 8, wherein the middle concentration source/drain region is formed by implanting boron in the semiconductor substrate at an accelerating voltage of about 40 KeV at a dose of $5x10^{13}/cm^2$.

27. (Previously Presented) A semiconductor device in accordance with claim 2, wherein the gate electrode has a thickness of about 2500 Å.

28. (Previously Presented) A semiconductor device in accordance with claim 1, wherein the source region is formed by implanting phosphorous in the semiconductor substrate at an accelerating voltage of about 40 KeV at a dose of $3.5x10^{13}/cm^2$.

29. (Previously Presented) A semiconductor device in accordance with claim 1, wherein the source region is formed by implanting phosphorous in the diffusion region at an accelerating voltage of about 40 KeV at a dose of $3.5x10^{13}/cm^2$ and by implanting arsenic at an accelerating voltage of about 80 KeV at a dose of $5x10^{15}/cm^2$, and the drain region is formed by implanting arsenic at an accelerating voltage of about 80 KeV at a dose of $5x10^{15}/cm^2$.

30. (Previously Presented) A semiconductor device in accordance with claim 1, wherein the drift region has an impurity concentration of about $1x10^{17}/cm^3$.

31. (Previously Presented) A semiconductor device in accordance with claim 17, wherein the size of the element isolation film is about 5 μm to 8 μm and a distance from an end of the element isolation film to the channel stopper layer is about 2 μm to 3 μm.

32. (Previously Presented) A semiconductor device in accordance with claim 17, wherein the channel stopper layer is formed in the semiconductor substrate by implanting boron at an accelerating voltage of about 60 KeV at a dose of $5x10^{13}/cm^2$.

33. (Previously Presented) A semiconductor device in accordance with claim 3, wherein the dopant concentration of said first part is higher than that of said second part.

34. (Previously Presented) A semiconductor device in accordance with claim 4, wherein the dopant concentration of said first part is higher than that of said second part.